Notice of Allowability	Application No.	Applicant(s)	
	09/997,888	GOYAL ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *June 14, 2005*.

2. ☒ The allowed claim(s) is/are *1 and 3-20*.

3. ☐ The drawings filed on _____ are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *Clean copy of allowed claims*.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' communication dated June 14, 2005. Claims 1 and 3 were amended. Claim 2 was deleted. Claim 20 was added. Claims 1, 3-20 of the application are pending.

Examiner's Amendment

2. Authorization for this examiner's amendment was given in a telephone conversation by Mr. Kelvin Vivian on August 26, 2005.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicants, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. In the claims:

In Claim 1, Line 2, "the method comprising the steps of"

has been changed to

-- the method comprising --

In Claim 3, Line 2, "into one global cone"

has been changed to

-- into one global clock cone --

Replace Claim 4 with:

4. The method of claim 3 further including:

(c) merging outputs from the instances of the delay prediction application into a final output file.

In Claim 5, Line 1, "The method of claim 4 further including step of using"

has been changed to

-- The method of claim 4 further including using --

In Claim 6, Line 1, "The method of claim 5 further including step of: running"

has been changed to

-- The method of claim 5 further including: running --

Replace Claim 7 with:

7. The method of claim 6 further including:

inputting output from the monolithic delay prediction application and the design cones into the respective instances of delay prediction application.

Replace Claim 8 with:

8. A method for predicting delay of a multi-million gate ASIC design, the method comprising:

(a) partitioning a netlist into timing-independent cones including a global clock cone and multiple design cones;

(b) performing delay calculation on the global clock cone and producing an output;

(c) performing delay calculation on the multiple design cones in parallel using as input the output from delay calculation on the global clock cone; and

(d) merging results from the delay calculations on the design cones and the delay calculation on the global clock cone into an output file.

In Claim 9, Line 1, "The method of claim 8 wherein step (a) further includes the step of"

has been changed to

-- The method of claim 8 wherein step (a) further includes --

In Claim 10, Line 1, "The method of claim 9 wherein step (b) further includes the step of"

has been changed to

-- The method of claim 9 wherein step (b) further includes --

In Claim 11, Line 1, "The method of claim 10 wherein step (b) further includes the step of"

has been changed to

-- The method of claim 10 wherein step (b) further includes --

Replace Claim 12 with:

12. The method of claim 11 wherein step (c) further includes:

(i) using an output file from the delay calculation on the global clock cone and the design cones as input to parallel instances of delay prediction application.

Replace Claim 13 with:

13. The method of claim 12 wherein step (c) further includes:

(ii) allocating one computer to run one instance of the delay prediction application, and using one instance of the delay prediction application to perform delay calculation on one design cone.

Replace Claim 14 with:

14. The method of claim 13 wherein step (c) further includes:

(iii) starting the instances of the delay prediction application on all computers at the same time and running the instances of the application in parallel so that delay output files for all design cones are produced at approximately the same time.

Replace Claim 15 with:

15. The method of claim 14 wherein step (d) further includes:

using scripts to merge the output file from the delay calculation on the global clock cone and the output files from the delay calculations on the design cones into a final output file.

Replace Claim 16 with:

16. A method for partitioning a netlist into timing-independent blocks of logic for distributed delay prediction, the method comprising:

(a) initializing all data structures related to cone traversal;

(b) finding a global clock cone;

(c) finding design cones;

(d) merging the design cones if a number of the design cones found is more than a number of computers available to perform the distributed delay prediction;

(e) creating a clock network;

(f) transforming the global clock cone into a writer cone and a write netlist;

(g) transforming the design cones into writer cones and write netlists; and

(h) generating for each cone a netlist, a prospective pin list file, and a force ramptime pin list file.

In Claim 17, Line 1, "The method of claim 16 further including step of"

has been changed to

-- The method of claim 16 further including --

In Claim 18, Line 1, "The method of claim 17 wherein step (e) further includes the step of"

has been changed to

-- The method of claim 17 wherein step (e) further includes --

Replace Claim 19 with:

19. The method of claim 18 wherein step (g) further includes:

transforming the design cones using multithreading.

Replace Claim 20 with:

20. The method of claim 4, wherein merging the outputs from the instances of the delay prediction application into the final output file includes merging each output into a standard delay format (SDF) output file.

A clean copy of the allowed claims is attached.

4. The following changes to the drawings have been approved by the examiner and agreed upon by applicant: See the agreed upon changes to Fig. 4 and Fig. 5 indicated by the red marked corrections.

In order to avoid abandonment of the application, applicant must make these above agreed upon drawing changes.

Reasons for Allowance

5. Claims 1, 3-20 of the application are allowed over prior art of record.

6. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) design tools that optimize area performance and signal integrity in integrated circuits; circuit partitioning to group highly connected portions of the design into clusters for subsequent layout; logic simulation and static timing analysis at gate level to verify functional behavior and estimate timing parameters; parallel placement algorithms executed by parallel processors, shortening the time to achieve placement functions; parallel processing systems include multiple central processors, executing independently of each other; parallel processing design automation system supports multithread execution; adapts algorithms for placement, timing analysis, logic optimization and routing suitable for parallel execution by multiple CPUs (**Boyle et al.,** U.S. Patent Application 2001/0010090);

(2) method of concurrently synthesizing different blocks of a circuit design using budgeting techniques for determining timing; partition large circuit design into smaller blocks to allow conventional synthesis tools to be used; establish a list of interconnected physical blocks out of a hierarchical netlist; groups of engineers work in parallel on synthesis of various blocks; timing allocation is performed by identifying logic cones from the gates of unoptimized netlist;

the logic cones are used to adjust the timing; use the cones to identify timing critical arcs (**Ginetti,** U.S. Patent 6,622,291); and

(3) logic synthesis performs netlist optimization based on performance estimates; a thread is a sequence of instructions with a single locus of control; multi-threaded programs have multiple control loci, implying parallelism; the design process creates a multithreaded description with parallelism; the computer may choose to execute threads in parallel on multiple CPUs or concurrently on one CPU, one thread after another; global clock spans the complete system; processor assignment assigns a thread to a processor and determines how the load will be distributed among a set of processors (**Vandeweerd,** U.S. Patent Application 2004/0006584).

None of these references taken either alone or in combination with the prior art of record discloses a method for predicting delay of a multi-million gate sub-micron ASIC design, specifically including:

"automatically partitioning a netlist into at least two timing-independent logic cones such that a timing effect of a first logic cone does not propagate to, or affect, a second logic cone in the design; and running respective instances of a delay prediction application on the timing-independent logic cones on at least two computers in parallel".

None of these references taken either alone or in combination with the prior art of record discloses a method for predicting delay of a multi-million gate ASIC design, specifically including:

"partitioning a netlist into timing-independent cones including a global clock cone and multiple design cones; performing delay calculation on the global clock cone; performing delay calculation on the multiple design cones in parallel; and merging results from the delay calculations on the design cones and the delay calculation on the global clock cone into an output file".

None of these references taken either alone or in combination with the prior art of record discloses a method for partitioning a netlist into timing-independent blocks of logic for distributed delay prediction, specifically including:

"finding a global clock cone; finding design cones; transforming the global clock cone into a writer cone and a write netlist; transforming the design cones into writer cones and write netlists; and generating for each cone a netlist, a prospective pin list file, and a force ramptime pin list file".

7. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is

571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard, can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

K. Thangavelu
Art Unit 2123
August 26, 2005

Paul L. Rodriguez 9/1/05
Primary Examiner
Art Unit 2125

Agreed upon changes to the Drawings

The attached red marked drawings show the agreed upon changes to Fig. 4 and Fig. 5.

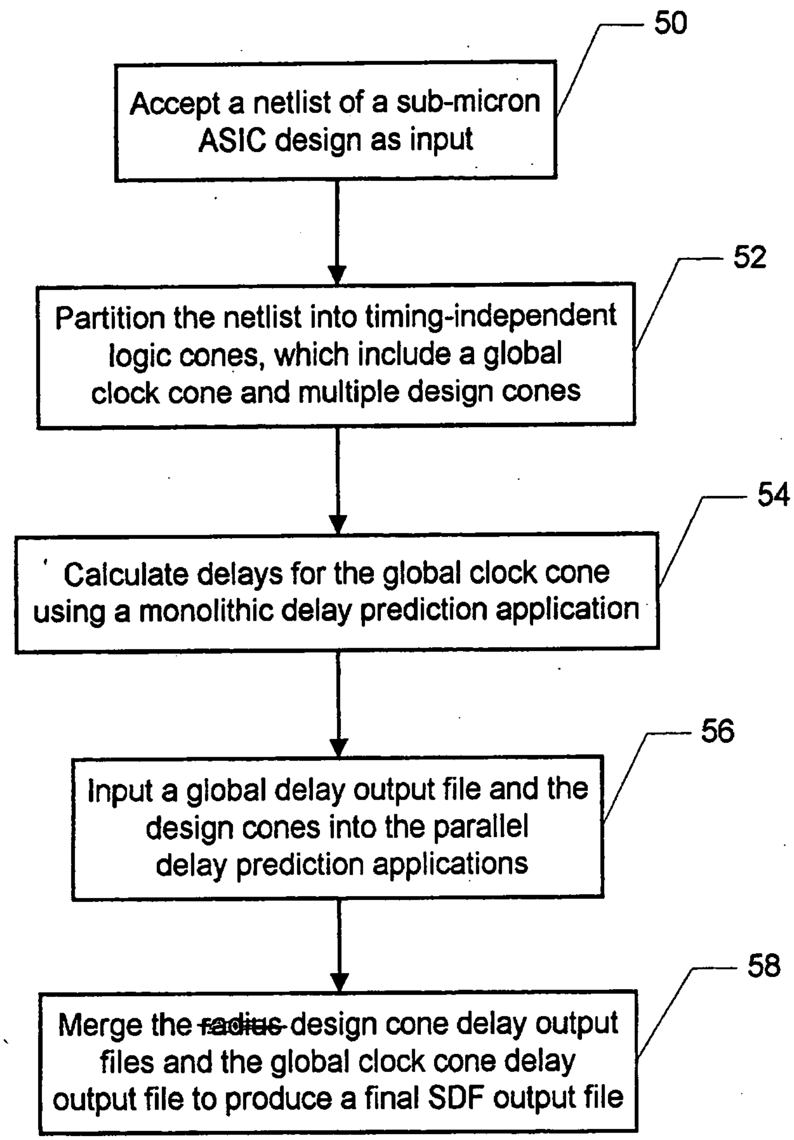
50
Accept a netlist of a sub-micron ASIC design as input
52
Partition the netlist into timing-independent logic cones, which include a global clock cone and multiple design cones
54
Calculate delays for the global clock cone using a monolithic delay prediction application
56
Input a global delay output file and the design cones into the parallel delay prediction applications
58
Merge the ~~radius~~ design cone delay output files and the global clock cone delay output file to produce a final SDF output file

FIG. 4

Serial No: 09/997,388
Group Art Unit: 2123
Replacement Sheet

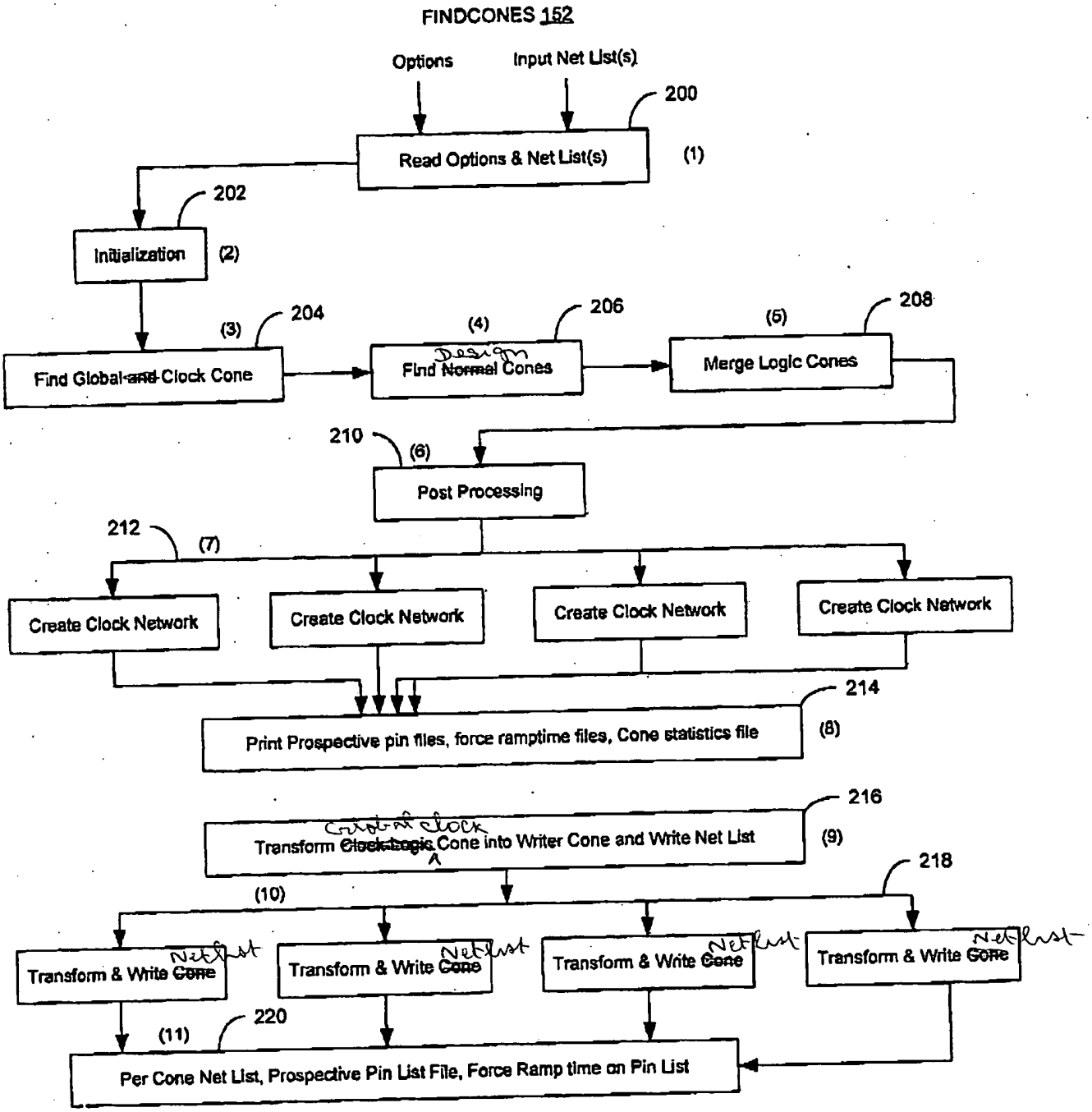

FIG. 5

Clean copy of the allowed claims

1. A method for predicting delay of a mufti-million gate sub-micron ASIC design, the method comprising:

(a) automatically partitioning a netlist into at least two timing-independent logic cones such that a timing effect of a first logic cone does not propagate to, or affect, a second logic cone in the design; and

(b) running respective instances of a delay prediction application on the timing-independent logic cones on at least two computers in parallel.

3. The method of claim 1 wherein partitioning the netlist includes partitioning the netlist into one global clock cone and multiple design cones.

4. The method of claim 3 further including:

(c) merging outputs from the instances of the delay prediction application into a final output file.

5. The method of claim 4 further including using a partitioning program to automatically partition the netlist.

6. The method of claim 5 further including:

running the global clock cone through a monolithic delay prediction application.

7. The method of claim 6 further including:

inputting output from the monolithic delay prediction application and the design cones into the respective instances of delay prediction application.

8. A method for predicting delay of a multi-million gate ASIC design, the method comprising:

(a) partitioning a netlist into timing-independent cones including a global clock cone and multiple design cones;

(b) performing delay calculation on the global clock cone and producing an output;

(c) performing delay calculation on the multiple design cones in parallel using as input the output from delay calculation on the global clock cone; and

(d) merging results from the delay calculations on the design cones and the delay calculation on the global clock cone into an output file.

9. The method of claim 8 wherein step (a) further includes:

(i) partitioning the netlist so that each of the multiple design cones includes approximately a same number of gates.

10. The method of claim 9 wherein step (b) further includes:

(i) forming the global clock cone by identifying clock networks, reset pins, and logic controlled by a clock throughout the ASIC design.

11. The method of claim 10 wherein step (b) further includes:

(ii) calculating delays for the global clock cone using a monolithic delay prediction application.

12. The method of claim 11 wherein step (c) further includes:

(i) using an output file from the delay calculation on the global clock cone and the design cones as input to parallel instances of delay prediction application.

13. The method of claim 12 wherein step (c) further includes:

(ii) allocating one computer to run one instance of the delay prediction application, and using one instance of the delay prediction application to perform delay calculation on one design cone.

14. The method of claim 13 wherein step (c) further includes:

(iii) starting the instances of the delay prediction application on all computers at the same time and running the instances of the application in parallel so that delay output files for all design cones are produced at approximately the same time.

15. The method of claim 14 wherein step (d) further includes:

using scripts to merge the output file from the delay calculation on the global clock cone and the output files from the delay calculations on the design cones into a final output file.

16. A method for partitioning a netlist into timing-independent blocks of logic for distributed delay prediction, the method comprising:

(a) initializing all data structures related to cone traversal;

(b) finding a global clock cone;

(c) finding design cones;

(d) merging the design cones if a number of the design cones found is more than a number of computers available to perform the distributed delay prediction;

(e) creating a clock network;

(f) transforming the global clock cone into a writer cone and a write netlist;

(g) transforming the design cones into writer cones and write netlists; and

(h) generating for each cone a netlist, a prospective pin list file, and a force ramptime pin list file.

17. The method of claim 16 further including:

(i) providing each netlist that was generated for each cone to one of the available computers, such that all of the available computers perform the delay prediction on the netlists in parallel.

18. The method of claim 17 wherein step (e) further includes:

creating the clock network using multithreading.

19. The method of claim 18 wherein step (g) further includes:

transforming the design cones using multithreading.

20. The method of claim 4, wherein merging the outputs from the instances of the delay prediction application into the final output file includes merging each output into a standard delay format (SDF) output file.